#32/Response (Not Okimg 8-27-03

Docket No. 0756-1974

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	Art Unit: 2822
Yasuhiko TAKEMURA et al.	)	Examiner: Mary A. Wilczewski
Serial No. 09/321,715	)	
Filed: May 28, 1999	)	
For: SEMICONDUCTOR DEVICE	)	
AND PROCESS FOR	)	
FABRICATING THE SAME	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with The United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 4, 2003.

RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Official Action mailed April 4, 2003, has been received and its contents carefully noted. Filed concurrently herewith is a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to August 4, 2003. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on May 28, 1999, April 4, 2000, and March 21, 2001.

Claims 1, 3-9, 11-17, 19-25, 27-33, 35-41, and 43-117 are pending in the present application, of which claims 1, 9, 17, 25, 33, 41, 49, 56, 63, 70, 78 and 86 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

The Official Action rejects claims 1-117 as obvious based on the combination of U.S. Patent No. 5,322,807 to Chen et al. and U.S. Patent No. 4,597,160 to Ipri, either alone or in combination with one or more of the following references: U.S. Patent No. 4,851,363 to Troxell et al., Wolf et al., "Silicon Processing for the VLSI Era, Volume 1: Process Technology," 1986, pp. 171-175 (Wolf I) and 216-218 (Wolf II). The Applicants